REMARKS

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

Claims 1, 6, 11, and 16 have been amended as shown above.

Claims 5 and 15 have been cancelled.

Claims 21 and 22 have been added.

Claims 1-4, 6-14, and 16-22 are now pending in this application.

Reconsideration and full allowance of Claims 1-4, 6-14, and 16-22 are respectfully requested.

I. OBJECTION TO CLAIMS

The Office Action objects to Claim 11 because the features of a "data processor" were recited under "a plurality of memory-mapped peripheral circuits." The Applicant has amended Claim 11 as suggested in the Office Action. The Applicant respectfully requests withdrawal of the objection.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-10 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,805,852 to Nakanishi et al. ("*Nakanishi*"). This rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if

every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Nakanishi recites a bypass control circuit for a processor. (*Abstract*). The bypass control circuit is capable of providing data from result buffers in execution stages (EX) and memory access stages (MEM) to latch circuits. (*Abstract; Figure 3*). The latch circuits then provide the data to arithmetic and logic units (ALU). (*Figure 3*). The processor also includes multiple buses (elements 1-1 through 4-2) that provide data to the latch circuits in the processor. (*Figure 3*). Each bus is associated with a particular one of the latch circuits. (*Figure 3*). In addition, the processor includes tri-state buffers (elements T1 through T72) that connect various sources of data to the buses. (*Figure 3*).

Nakanishi simply recites a mechanism for using tri-state buffers to supply a particular data value to a specific bus, thereby providing the data value to a specific latch circuit in the processor of *Nakanishi*. *Nakanishi* lacks any mention of using multiplexers with the tri-state buffers. Because of this, this portion of *Nakanishi* fails to anticipate a "data processor" that includes "bypass circuitry," where the bypass circuitry includes a "plurality of bypass tristate line drivers" and a "multiplexer" as recited in Claim 1.

In discussing a "conventional scalar processor," *Nakanishi* recites the use of multiplexers. (*Col. 3, Lines 19-20; Figure 28*). However, the conventional processor shown in Figure 28 of

Nakanishi contains no tri-state buffers. As a result, there is no recitation in *Nakanishi* of using multiplexers with the tri-state buffers. In fact, the tri-state buffers of *Nakanishi* ensure that only one data value is supplied to any single bus in the processor at any particular time, so there is no actual need for multiplexers in the processor of *Nakanishi*. Because of this, this portion of *Nakanishi* fails to recite "bypass circuitry" that includes both a "plurality of bypass tristate line drivers" and a "multiplexer" as recited in Claim 1.

For these reasons, *Nakanishi* fails to anticipate the Applicant's invention as recited in Claim 1 (and its dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 1-10.

III. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 11-20 under 35 U.S.C. § 103(a) as being unpatentable over *Nakanishi* in view of U.S. Patent No. 4,591,973 to Ferris, III et al. ("*Ferris*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce

evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

As described above in Section II, the Office Action does not establish that *Nakanishi* discloses, teaches, or suggests various elements of Claim 1. The Office Action therefore also does not establish that *Nakanishi* discloses, teaches, or suggests analogous elements recited in Claim 11. In addition, the Office Action does not show that *Ferris* discloses, teaches, or suggests these elements of Claim 11. As a result, the Office Action has not shown that the

proposed *Nakanishi-Ferris* combination discloses, teaches, or suggests all elements of Claim 11.

For these reasons, the Office Action has not shown that the proposed *Nakanishi-Ferris* combination discloses, teaches, or suggests the Applicant's invention as recited in Claim 11 (and its dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 11-20.

IV. CONCLUSION

As a result of the foregoing, the Applicant asserts that all pending claims in the application are in condition for allowance and respectfully requests an early allowance of such claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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